CLAIMS

What is claimed is:

1. In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity;

coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; and

altering the first capacity and the second capacity during the operation of the memory system.

2. The method of claim 1 wherein the acts of altering the first capacity and the second capacity comprise altering the first capacity and the second capacity based on the rate at which the signals are being coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which the signals are being coupled from the memory hub in the at least one memory module to the module memory hub controller.

3. The method of claim 2 wherein the acts of altering the first capacity and the second capacity comprise:

at the memory hub controller, determining the rate at which the signals are being coupled between the memory hub controller and the memory hub in the at least one memory module; and

altering the first capacity and the second capacity based on the determined rate at which the signals are being coupled between the memory hub controller and the memory hub in the at least one memory module.

4. The method of claim 2 wherein the acts of altering the first capacity and the second capacity comprise:

at the memory hub of the at least one memory module, determining the rate at which the signals are being coupled between the memory hub controller and the memory hub; and

altering the first capacity and the second capacity based on the determined rate at which the signals are being coupled between the memory hub controller and the memory hub.

5. The method of claim 2 wherein the acts of altering the first capacity and the second capacity comprise:

using software to determine the rate at which the signals are being coupled between the memory hub controller and the memory hub of the at least one memory module; and

altering the first capacity and the second capacity based on the rate determined by the software.

6. The method of claim 5 wherein the act of using software to determine the rate at which the signals are being coupled between the memory hub controller and the memory hub of the at least one memory module comprises using operating system software to determine the rate at which the signals are being coupled

between the memory hub controller and the memory hub of the at least one memory module.

7. The method of claim 2 wherein the acts of altering the first capacity and the second capacity comprise:

determining the rate at which the signals are being coupled between the memory hub controller and the memory hub of the at least one memory module at a location other than the memory hub of the at least one memory module;

transmitting information indicative of the determined rate to the memory hub of the at least one memory module; and

altering the first capacity and the second capacity based on the transmitted information.

8. The method of claim 2 wherein the acts of altering the first capacity and the second capacity comprise:

determining the rate at which the signals are being coupled between the memory hub controller and the memory hub of the at least one memory module at a location other than the memory hub controller;

transmitting information indicative of the determined rate to the memory hub controller; and

altering the first capacity and the second capacity based on the transmitted information.

9. The method of claim 1 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise configuring buffers in the memory hub controller and in the memory hub of the at least one memory module as either input buffers or output buffers.

10. The method of claim 1 wherein the acts of altering the first capacity and the second capacity comprise altering the first capacity and the second capacity based on the rate at which it is anticipated that the signals will be coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which it is anticipated that the signals will be coupled from the memory hub in the at least one memory module to the module memory hub controller.

11. The method of claim 10 wherein the acts of altering the first capacity and the second capacity comprise:

determining the rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module based on the type of hardware included in a system associated with the memory system; and

altering the first capacity and the second capacity based on the determined rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module.

12. The method of claim 1 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity within a range of minimum and maximum values for the first capacity and the second capacity.

13. The method of claim 1 wherein the acts of altering the first capacity and the second capacity comprise manually altering the first capacity and the second capacity.

14. The method of claim 13 wherein the acts of manually altering the first capacity and the second capacity comprise manually adjusting at least one electrical connection.

15. The method of claim 1 wherein the act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module comprises coupling a packet containing command, address and data signals from the memory hub controller to the memory hub in the at least one memory module.

16. The method of claim 1 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity during the initialization of the memory system.

17. In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having a M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus;

coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M; and

altering the values of N and P during the operation of the memory system.

18. The method of claim 17 wherein the acts of altering the first number of signal lines and the second number of signal lines comprise altering the values of N and P based on the rate at which signals are being coupled through the bus.

19. The method of claim 18 wherein the acts of altering the values of N and P comprise:

at the memory hub controller, determining the rate at which the signals are being coupled through the bus; and

altering the values of N and P based on the determined rate at which the signals are being coupled through the bus.

20. The method of claim 18 wherein the acts of altering the values of N and P comprise:

at the memory hub of the at least one memory module, determining the rate at which the signals are being coupled through the bus; and

altering the values of N and P based on the determined rate at which the signals are being coupled through the bus.

21. The method of claim 18 wherein the acts of altering the values of N and P comprise:

using software to determine the rate at which the signals are being coupled through the bus; and

altering the values of N and P based on the rate determined by the software.

22. The method of claim 21 wherein the act of using software to determine the rate at which the signals are being coupled through the bus comprises using operating system software to determine the rate at which the signals are being coupled through the bus.

23. The method of claim 18 wherein the acts of altering the values of N and P based on the rate at which the signals are being coupled through the bus comprise altering the values of N and P based on the rate at which the signals are being coupled through the bus from the memory hub controller to the memory hub in the at least one memory module.

24. The method of claim 18 wherein the acts of altering the values of N and P based on the rate at which the signals are being coupled through the bus comprise altering the values of N and P based on the rate at which the signals are being coupled through the bus from the memory hub in the at least one memory module to the memory hub controller.

25. The method of claim 18 wherein the acts of altering the values of N and P comprise:

determining the rate at which the signals are being coupled through the bus at a location other than the memory hub of the at least one memory module;

transmitting information indicative of the determined rate to the memory hub of the at least one memory module; and

altering the altering the values of N and P based on the transmitted information.

26. The method of claim 18 wherein the acts of altering the values of N and P comprise:

determining the rate at which the signals are being coupled through the bus at a location other than the memory hub controller;

transmitting information indicative of the determined rate to the memory hub controller; and

altering the altering the values of N and P based on the transmitted information.

27. The method of claim 17 wherein the acts of altering the values of N and P during the operation of the memory system comprise configuring buffers in the memory hub controller and in the memory hub of the at least one memory module as either input buffers or output buffers.

28. The method of claim 18 wherein the acts of altering the values of N and P comprise altering the altering the values of N and P based on the rate at which it is anticipated that the signals will be coupled through the bus.

29. The method of claim 28 wherein the acts of altering the values of N and P comprise:

determining the rate at which it is anticipated that the signals will be coupled through the bus; and

altering the values of N and P based on the determined rate at which it is anticipated that the signals will be coupled through the bus.

30. The method of claim 17 wherein the acts of altering the values of N and P during the operation of the memory system comprise altering the values of N and P within a range of minimum and maximum values of N and P.

31. The method of claim 17 wherein the acts of altering the values of N and P comprise manually altering the values of N and P.

32. The method of claim 31 wherein the act of manually altering the values of N and P comprise manually adjusting at least one electrical connection.

33. The method of claim 17 wherein the act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus comprises coupling a packet containing command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus.

34. The method of claim 17 wherein act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus comprises coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a uni-directional downstream bus having N signal lines, and wherein the act of coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus comprise coupling comprises coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a uni-directional upstream bus having P signal lines.

35. The method of claim 17 wherein the acts of altering the values of N and P during the operation of the memory system comprise altering the values of N and P during the initialization of the memory system.

36. A memory system, comprising:

a memory hub controller having M buffers, N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, the values of N and P being alterable during the operation of the memory system;

at least one memory module, comprising

a memory hub having a plurality of buffers, N of which are configured as input buffers and P of which are configured as output buffers; and

a plurality of memory devices coupled to the memory hub; and

a bus having M signal lines each of which is coupled between a respective buffer of the memory hub controller and a respective buffer of the memory hub, the value of M being equal to the sum of N and P.

37. The memory system of claim 36 wherein the values of M and N for the buffers in the memory hub controller and the memory hub are altered based on the rate at which the signals are being coupled through the bus.

38. The memory system of claim 37 wherein the memory hub controller is operable to determine the rate at which the signals are being coupled through the bus, and wherein the values of M and N for the buffers in the memory hub controller and the memory hub are altered based on the determined rate at which the signals are being coupled through the bus.

39. The memory system of claim 37 wherein the memory hub is operable to determine the rate at which the signals are being coupled through the bus, and wherein the values of M and N for the buffers in the memory hub controller and the memory hub are altered based on the determined rate at which the signals are being coupled through the bus.

40. The memory system of claim 37 wherein the values of M and N for the buffers in the memory hub controller and the memory hub are altered based on the rate at which the signals are being coupled through the bus from the memory hub controller to the memory hub.

41. The memory system of claim 37 wherein the values of M and N for the buffers in the memory hub controller and the memory hub are altered based on the rate at which the signals are being coupled through the bus from the memory hub to the memory hub controller.

42. The memory system of claim 36 wherein the values of M and N for the buffers in the memory hub controller and the memory hub are altered based on the rate at which it is anticipated that the signals will be coupled through the bus.

43. The memory system of claim 42 wherein the memory hub controller is operable to determine the rate at which it is anticipated that the signals will be coupled through the bus, and wherein the values of M and N for the buffers in the memory hub controller and the memory hub are altered based on the determined rate at which it is anticipated that the signals will be coupled through the bus.

44. The memory system of claim 42 wherein the memory hub is operable to determine the rate at which it is anticipated that the signals will be coupled through the bus, and wherein the values of M and N for the buffers in the memory hub controller and the memory hub are altered based on the determined rate at which it is anticipated that the signals will be coupled through the bus.

45. The memory system of claim 36 wherein the values of N and P are altered within a range of minimum and maximum values of N and P.

46. The memory system of claim 36 wherein the memory hub controller is operable to alter the values of N and P during initialization of the memory system.

47. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port;

a memory hub controller coupled to the processor bus, the memory hub controller having an output port and an input port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller;

at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub;

a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus having a width of M bits, the value of M being variable to adjust that bandwidth of the downstream bus; and

an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth of the upstream bus.

48. The processor-based system of claim 47 wherein the values of M and N are altered based on the rate at which the signals are being coupled through at least one of the downstream bus and the upstream bus.

49. The processor-based system of claim 48 wherein the memory hub controller is operable to determine the rate at which the signals are being coupled through at least one of the downstream bus and the upstream bus, and wherein the values of M and N are altered based on the determined rate at which the signals are being coupled through at least one of the downstream bus and the upstream bus.

50. The processor-based system of claim 48 wherein the memory hub is operable to determine the rate at which the signals are being coupled through at least one of the downstream bus and the upstream bus, and wherein the values of M and N are altered based on the determined rate at which the signals are being coupled through at least one of the downstream bus and the upstream bus.

51. The processor-based system of claim 48 wherein the values of M and N are altered based on the rate at which the signals are being coupled through the downstream bus from the memory hub controller to the memory hub.

52. The processor-based system of claim 48 wherein the values of M and N are altered based on the rate at which the signals are being coupled through the upstream bus from the memory hub to the memory hub controller.

53. The processor-based system of claim 47 wherein the values of M and N are altered based on the rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus.

54. The processor-based system of claim 53 wherein the memory hub controller is operable to determine the rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus, and wherein the values of M and N are altered based on the determined rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus.

55. The processor-based system of claim 53 wherein the memory hub is operable to determine the rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus, and wherein the values of M and N are altered based on the determined rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus.

56. The processor-based system of claim 47 wherein the values of N and P are altered within a range of minimum and maximum values of N and P.

57. The processor-based system of claim 47 wherein the values of N and P are altered during initialization of the processor-based system.